L	Hits	Search Text	DB	Time stamp
Number	165	712/206.ccls.	USPAT	2004/11/03
	165	/12/206.CCIs.	USPAT	09:45
2	292	712/208.ccls.	USPAT	2004/11/03
3	218	712/209.ccls.	USPAT	2004/11/03
4	212	712/213.ccls.	USPAT	2004/11/03
5	351	712/210.ccls.	USPAT	2004/11/03 09:45
6	47	(width near4 bits) with instruction with	USPAT; EPO; JPO	2004/11/03
7	89	(width size length) with instruction with (signal indicat\$4) with bit with decoder	USPAT; EPO; JPO	2004/11/03
8	6	bits with instruction with size with indicat\$4 with width	USPAT; EPO; JPO	2004/11/03
9	32	emulation near3 ("instruction register"	USPAT; EPO; JPO	2004/11/03
10	126	(decod\$4 near4 priority) with instruction	USPAT; EPO; JPO	2004/11/03
12	7	(emulation near3 ("instruction register" IR)) and ((decod\$4 near4 priority) with	USPAT; EPO; JPO	2004/11/03
13	50	instruction) decoder with width with bit with	USPAT;	2004/11/03
15	99	instruction multiplexor with decoder with instruction	EPO; JPO USPAT;	09:45 2004/11/03 09:46
11	9	(US-6182280-\$ or US-6110225-\$ or US-6449712-\$ or US-5941980-\$ or	EPO; JPO USPAT	09:46 2004/11/03 09:46
		US-5931944-\$ or US-5920713-\$ or US-5832258-\$ or US-5809272-\$ or US-6260134-\$ or US-5845102-\$).did.		
16	20	multiplexor with decoder with instruction with input	USPAT; EPO; JPO	2004/11/03 09:46
17	180	instruction with cache with bypass	USPAT; EPO; JPO	2004/11/03 09:46
14	19	speculative with ("instruction register")	USPAT	2004/11/03 09:46
18	123	instruction with cache with bypass	USPAT; EPO; JPO	2004/11/03 09:46
19	5	("instruction cache" with bypass) same decoder	USPAT; EPO; JPO	2004/11/03 09:46
20	13	(instruction with cache with bypass) same decoder	USPAT; EPO; JPO	2004/11/03 09:46
23	112	instruction with cache with bypass	USPAT	2004/11/03
21	5	("instruction cache" with bypass) same decoder	USPAT	2004/11/03 09:46
22	13	(instruction with cache with bypass) same decoder	USPAT	2004/11/03 09:46
-	13074	width near4 bits	USPAT	2003/09/24 14:12
-	527	(width near4 bits) with instruction	USPAT	2003/09/24 16:09
-	39	(width near4 bits) with instruction with size	USPAT	2004/04/13 16:16
-	171	bits with instruction with size with indicat\$4	USPAT	2003/09/24 14:22
-	5	bits with instruction with size with indicat\$4 with width	USPAT	2004/04/13 16:16
-	795	plurality with source with decoder	USPAT	2003/09/24 15:18
-	59	plurality near3 source near3 decoder	USPAT	2004/04/13 16:16
-	3	(plurality near3 source near3 decoder) with instruction	USPAT	2003/09/24 15:58
-	86	instruction with decoder with multiplexor	USPAT	2004/04/13 16:16
-	0	(width near4 bits) with instruction with decoder with (mux multiplexor)	USPAT	2003/09/24 16:09
				·····

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-	1	(width near4 bits) same (instruction with	USPAT	2003/09/24
		decoder with (mux multiplexor))		16:11
-	2	(width near4 bits) same (instruction with	USPAT	2003/09/24
		decoder) same (mux multiplexor)		16:12
-	34	(width size length) same (instruction	USPAT	2003/09/24
		with decoder) same (mux multiplexor)		16:16
-	2983	(width size length) with instruction with	USPAT	2003/09/24
1		(signal indicat\$4)		16:17
-	746	(width size length) with instruction with	USPAT	2003/09/24
		(signal indicat\$4) with bit		16:17
-	74	(width size length) with instruction with	USPAT	2004/04/13
		(signal indicat\$4) with bit with decoder		16:16
-	0	(width size length) with instruction with	USPAT	2003/09/24
		(signal indicat\$4) with bit with decoder with (multiplexor mux)		16:17
	1	I	USPAT	2003/09/24
-	1	with (signal indicat\$4) with bit with	OSFAI	16:17
		decoder) same (multiplexor mux)		[10.17
	6	5809272.URPN.	USPAT	2003/09/24
		300 32 72 : OREW.	051111	17:11
l _	2	((US-6182280-\$ or US-6110225-\$ or	USPAT	2003/09/25
		US-6449712-\$ or US-5941980-\$ or	001111	12:05
		US-5931944-\$ or US-5920713-\$ or		
		US-5832258-\$ or US-5809272-\$ or		
1		US-6260134-\$ or US-5845102-\$).did.) and		
		dsp		
-	103	(decod\$4 near4 priority) with instruction	USPAT	2004/04/13
1				16:16
-	8	((decod\$4 near4 priority) with	USPAT	2003/09/26
		instruction) and dsp		16:25
_	3	((decod\$4 near4 priority) with	US-PGPUB	2003/09/26
		instruction) and dsp		16:25
-	17	emulation near3 "instruction register"	USPAT	2004/04/13
				16:16
-	7	(emulation near3 ("instruction register"	USPAT	2004/04/13
		IR)) and ((decod\$4 near4 priority) with		16:15
		instruction)		
-	0	"emulation instruction register"	USPAT	2003/09/26
	_			16:33
-	0	"emulation ir"	USPAT	2003/09/26
		2 /81 / 2 /81	**************************************	16:33
-	26	,	USPAT	2004/04/13
	0267	IR)	USPAT	2003/09/26
_	2367	(plural\$4 multiple) with ("instruction register" IR)	OSEVI	16:44
_	708		USPAT	2003/09/26
	'00	register")	332711	16:44
_	99	instruction with decoder with multiplexor	USPAT;	2004/10/29
			EPO; JPO	16:42
_	68	plurality near3 source near3 decoder	USPAT;	2004/10/29
			EPO; JPO	16:42
_	99	instruction with decoder with multiplexor	USPAT;	2004/10/29
			EPO; JPO	16:42
_	287	(plural\$4 multiple) near3 ("instruction	USPAT	2004/10/29
		register")		16:42
-	125	(decod\$4 near4 priority) with instruction	USPAT;	2004/10/29
			EPO; JPO	16:42
-	20	emulation near3 "instruction register"	USPAT;	2004/10/29
			EPO; JPO	16:42
-	2	((plural\$4 multiple) near3 ("instruction	USPAT	2004/10/29
		register")).ti.	IIGD? II	16:42
-	1	5721855.pn.	USPAT	2004/10/29
	_	/	IICDAM	17:02
-	0	(multiplexor with decoder with	USPAT	2004/10/29
		instruction) and (decoder with width with		17:02
	37	bit)	IISDAT	2004/10/29
-	37	decoder with width with bit with instruction	USPAT	18:14
_	99		USPAT	2004/10/29
-	39	mutciplexor with decoder with instruction	USEAT	18:14
_	20	multiplexor with decoder with instruction	USPAT	2004/10/29
	20	with input	33171	18:14
L	L	Laten tuhan	L	1 -0 - 1

i	169	instruction with	cache with	hunsee	USPAT	2004/10/29	
ŀ	100	Instruction with	Cacife with	Dypass	ODIAL	2004/10/29	
						18:14	
						10:14	